Application Note

NOVOSENSE

Introduction to CAN Dynamic Parameters and Effects on System Applications

AN-13-0013

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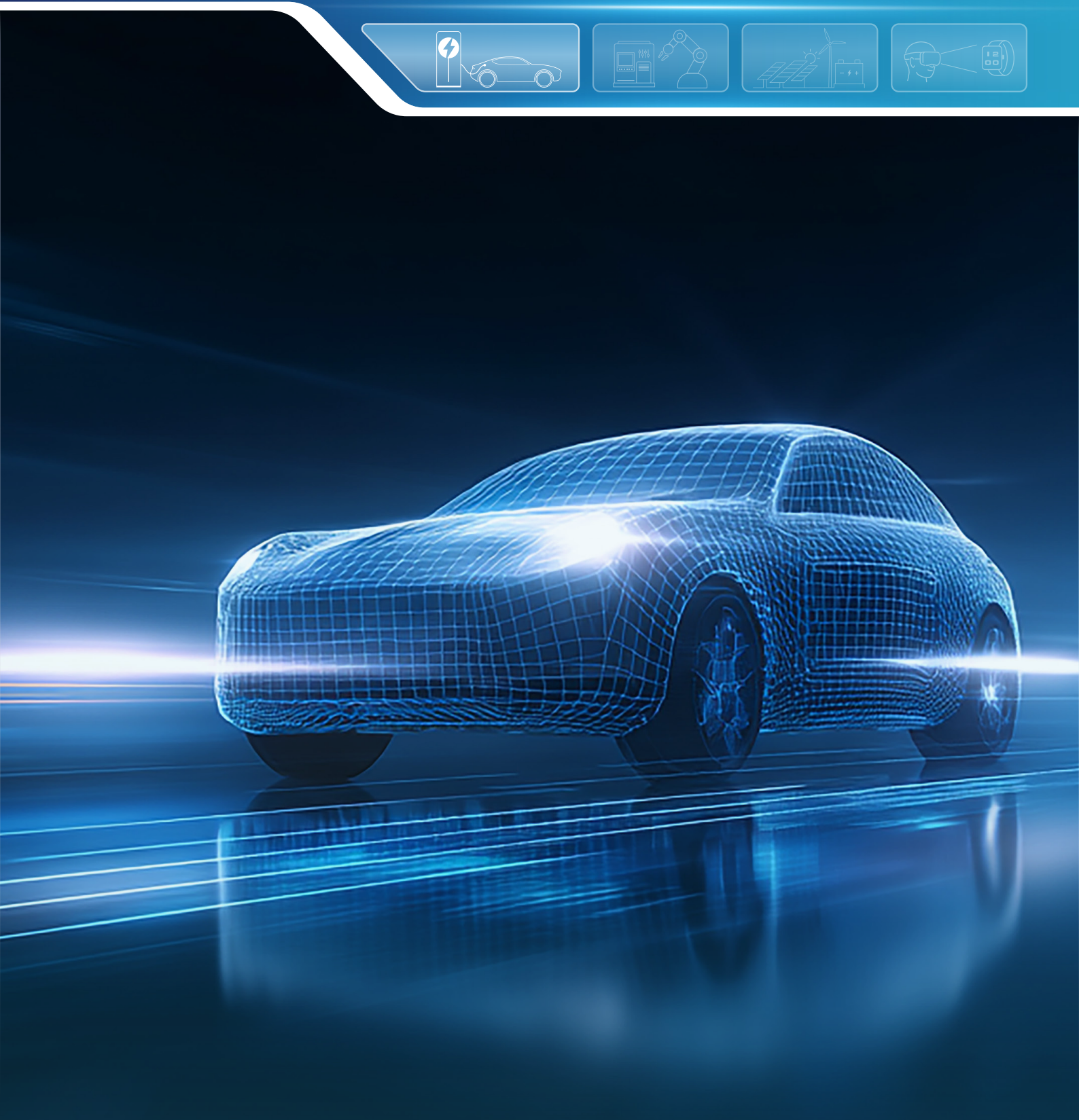

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ABSTRACT

The Controller Area Network (CAN) bus, as the most common serial communication protocol in automotive communication systems, is widely used for real-time data exchange between electronic control units (ECUs). In a vehicle network, dozens or even hundreds of CAN nodes are typically required for data exchange between vehicle modules. This poses more demanding requirements for CAN interface ICs regarding reliability, real-time performance, and interference immunity. NOVOSENSE has launched a series of CAN transceivers designed to meet the diverse CAN interface requirements across modern vehicle applications. This application note primarily discusses the effects of relevant CAN timing parameters on system applications.

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1.CAN Dynamic Parameters

The ISO11898-2 standard specifies physical layer parameters for CAN transceivers, including static electrical parameters and dynamic timing parameters. Key dynamic timing parameters include CAN propagation delay and bit-related timing parameters, which directly decides whether normal CAN communication is possible. When aligned with the requirements of the CAN protocol layer, these dynamic timing parameters enable normal operation of multi-node, long-bus CAN networks. This section details several key dynamic timing parameters related to CAN.

1.1.Rise/fall time

Although the ISO 11898-2 standard does not explicitly define rise/fall time parameters for CAN signals, these parameters significantly affect CAN communication in actual applications (discussed in detail in Section 3). The rise/fall time of a CAN signal mainly includes the rise/fall time of bus differential voltage (V_{dif}) and the rise/fall time of the output signal on the RXD pin. The TXD pin, being an input for external signals, will not be discussed here.

The general definition of CAN signal rise/fall time is shown in Figure 1.1:

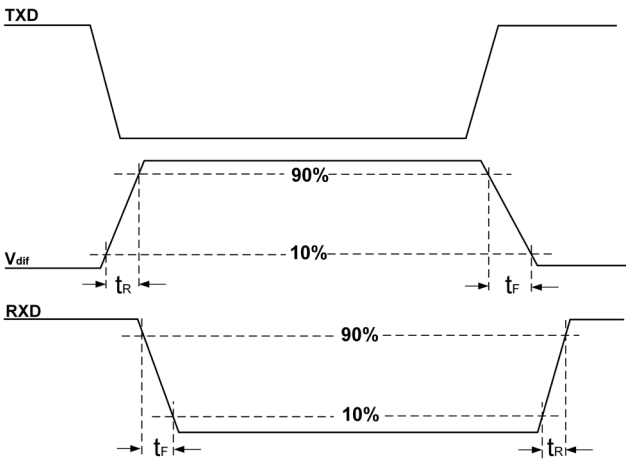
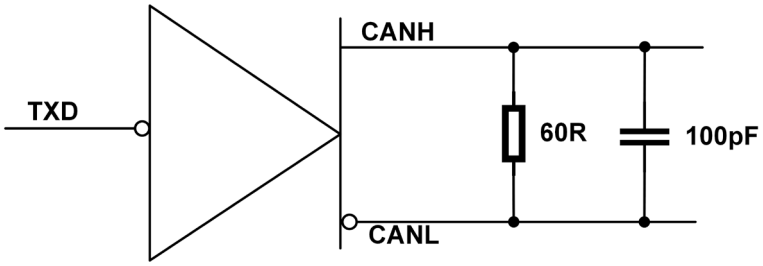
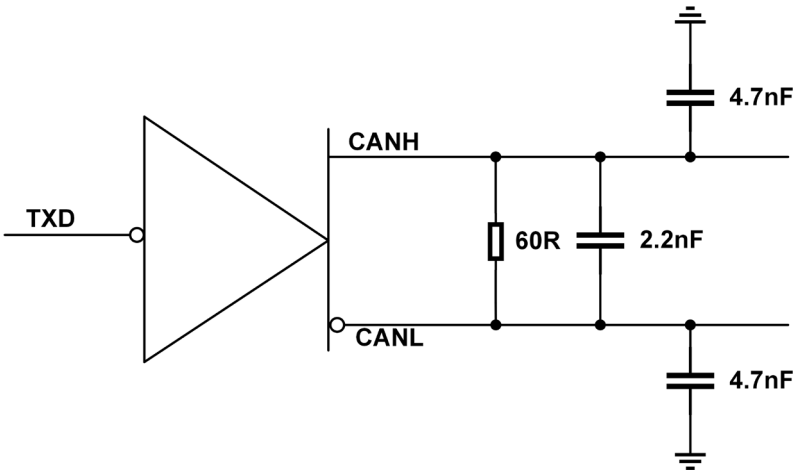


Figure 1.1 rise/fall time definition

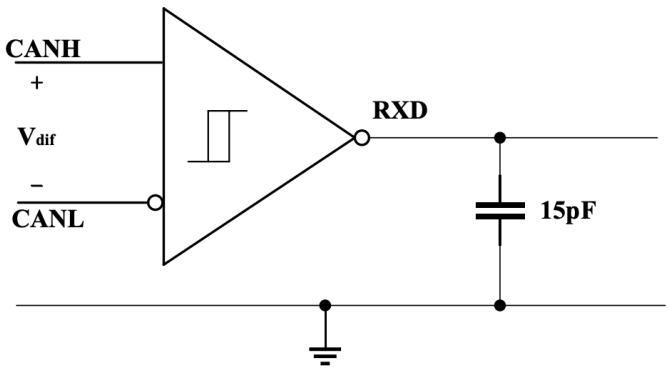
Below are the rise/fall time test results of NCA1044, NCA1462, NCA1043B, and NCA1145B from NOVOSENSE under different test setups, compared with corresponding mainstream devices from two international competitors. The test circuits are shown in Figure 1.2.



(a) Bus test circuit 1



(b) Bus test circuit 2



(c) RXD test circuit

Figure 1.2 Schematics of test circuits

The comparative test results are given below:

Table1 Comparison of rise/fall time in Circuit 1

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
t_R	36.35	34.44	22.2	22.24	39.02	10.54	29.68	35.46	35.06	34.71	60.24	25.54
t_F	49.19	42.9	44.67	26.14	25.88	15.75	30.72	41.23	51.06	45.87	52.69	51.11

Table2 Comparison of rise/fall time in Circuit 2

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
t_R	348.8	382.6	376	346.4	271.9	365.1	377.4	384.4	399.9	275	485.7	286.7
t_F	597	661	652.1	495	395.6	453.6	562.1	650.5	607.7	590.5	661.4	653.3

Table3 Comparison of rise/fall time in Circuit 3

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
t_R	5.69	3.1	7.874	3.669	7.388	5.688	9.6	2.856	3.471	5.599	5.589	2.379
t_F	6.89	3.57	6.256	4.755	5.938	5.96	7.33	2.718	2.508	4.253	5.631	1.967

1.2.Loop delay

The ISO11898-2 standard explicitly defines loop delay requirements. For a typical CAN transceiver, loop delay comprises transmission delay from TXD to the bus, transmission delay from the bus to RXD, and loop delay from TXD to RXD. Their specific definitions are shown in Figure 1.3.

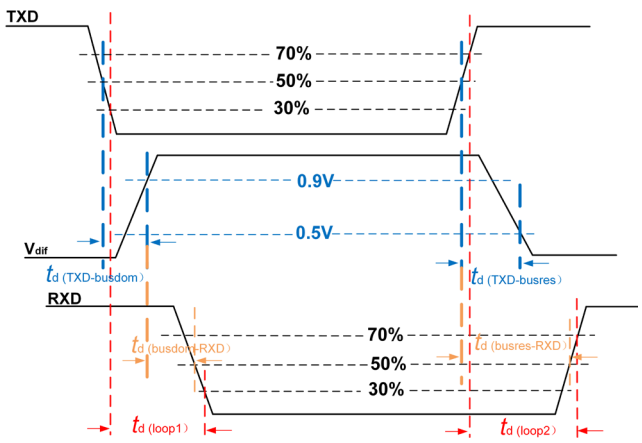


Figure 1.3 CAN propagation delay definition

Below are comparative test results of loop delay ($t_{d(loop)}$) for NCA1044, NCA1462, NCA1043B, and NCA1145B from NOVOSENSE under identical test conditions, benchmarked against corresponding mainstream devices from two international competitors. The test circuits are shown in Figure 1.2 (a) and (c).

The comparative test results are as follows:

Table 4 Comparison of $t_{d(loop1)}$test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{d(loop1)}$	125.7	105.9	115.1	121	134.2	91.29	137.1	122.9	127.9	125.6	176.4	120.8

Table 5 Comparison of $t_{d(loop2)}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{d(loop2)}$	147.1	141.4	141.7	128.7	135.9	98.38	160.7	141.1	138.6	146.8	218.6	151.6

Table 6 Comparison of $t_{d(TXD-busdom)}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{d(TXD-busdom)}$	40.15	33.02	53.55	42.26	58.56	43.13	53.29	47.09	39.38	40.31	61.84	54.92

Table7 Comparison of $t_{d(TXD-busres)}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{d(TXD-busres)}$	62.40	57.15	67.87	44.90	62.98	37.31	66.37	59.99	50.13	61.87	76.15	68.6

Table8 Comparison of $t_{d(busdom-RXD)}$ test results

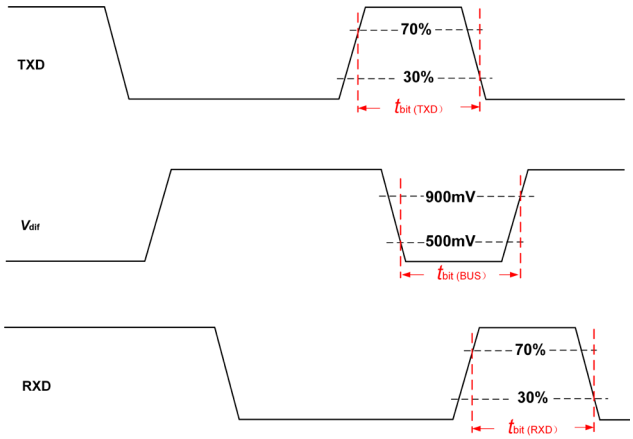
/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{d(busdom-RXD)}$	85.59	72.92	61.77	78.69	75.62	48.16	83.84	75.85	88.56	85.33	114.6	65.88

Table9 Comparison of $t_{d(busres-RXD)}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{d(busres-RXD)}$	84.73	84.27	73.81	83.84	72.94	61.08	94.37	81.12	88.5	84.88	142.5	83.01

1.3.Bit timing parameters

ISO11898-2 also specifies requirements for CAN transceiver bit timing parameters, which characterize the distortion of bit time as a CAN frame is transmitted through the transceiver. These parameters are crucial for maintaining reliable communication in CAN systems. Key bit timing parameters include bit time from TXD to the bus ($t_{bit(bus)}$), bit time distortion during transmission ($t_{\Delta bit(BUS)}$), bit time from the bus to RXD ($t_{bit(RXD)}$), bit time distortion during reception ($t_{\Delta REC}$), and bit time distortion from TXD to RXD ($t_{\Delta bit(RXD)}$), as illustrated in Figure 1.4.



Note:

$t_{\Delta bit(BUS)} = t_{bit(BUS)} - t_{bit(TXD)}$

$t_{\Delta bit(RXD)} = t_{bit(RXD)} - t_{bit(TXD)}$

$t_{\Delta Rec} = t_{bit(RXD)} - t_{bit(Bus)}$

Figure 1.4 bit timing definition

Below are comparative test results of bit timing parameters for NCA1044, NCA1462, NCA1043B, and NCA1145B from NOVOSENSE under identical test conditions, compared with corresponding mainstream devices from international competitors. The test setups are shown in Figure 1.2(a) and (c).

Table10 Comparison of $t_{bit(BUS)—5Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{bit(BUS)}$	192.5	192.8	197.5	198.2	195.2	206.2	187	188.4	191.4	179.5	185.2	186.3

Table11 Comparison of $t_{bit(BUS)—2Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{bit(BUS)}$	492.5	492.7	497.3	498.5	496.4	506.4	488.7	487.8	491.2	479.6	485.8	486.7

Table12 Comparison of $t_{bit(RXD)—5Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{bit(BUS)}$	179.8	163.9	172.3	193.2	198.3	193.2	177.2	183.5	193.9	180.3	155.3	172.3

Table13 Comparison of $t_{bit(RXD)—2Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{bit(RXD)}$	479.4	464.6	473.2	493	498.3	493.4	477.6	482.1	494	480.1	456.6	470.9

Table14 Comparison of $t_{\Delta bit(BUS)—5Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{\Delta bit (BUS)}$	-7.4	-7.2	-2.5	-1.8	-4.8	6.2	-12.9	-11.6	-8.6	-20.5	-14.8	-13.7

Table15 Comparison of $t_{\Delta bit(BUS)—2Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{\Delta bit (BUS)}$	-7.4	-7.2	-2.7	-1.5	-3.5	6.5	-13.3	-12.1	-8.7	-20.6	-14.1	-13.3

Table16 Comparison of $t_{\Delta REC—5Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{\Delta REC}$	-12.7	-28.9	-25.2	-5	2.9	-13	-9.8	-4.9	2.5	0.8	-29.9	-14

Table17 Comparison of $t_{\Delta REC—2Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{\Delta REC}$	-13.1	-28.1	-24.1	-5.5	1.9	-13	-11.1	-5.7	2.8	0.5	-29.2	-15.8

Table18 Comparison of $t_{\Delta bit(RXD)-5Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{\Delta bit(RXD)}$	-20.1	-36.1	-27.7	-6.8	-1.7	-6.8	-22.7	-16.5	-6.1	-19.7	-44.7	-27.7

Table19 Comparison of $t_{\Delta bit(RXD)-2Mbps}$ test results

/ns	NCA1044	Competitor 1	Competitor 2	NCA1462	Competitor 1	Competitor 2	NCA1043B	Competitor 1	Competitor 2	NCA1145B	Competitor 1	Competitor 2
$t_{\Delta bit(RXD)}$	-20.5	-35.3	-26.8	-7	-1.6	-6.5	-24.4	-17.8	-5.9	-20.1	-43.3	-29.1

All data above are derived from measured results obtained under identical laboratory conditions. Original waveform data is available upon request. Please contact your NOVOSENSE sales representatives.

2.CAN Sampling Principle

In system applications, the MCU of each ECU samples and processes the incoming CAN frames transmitted via the CAN transceiver according to predefined rules, and generates corresponding responses, thereby enabling reliable communication across the multi-node CAN bus network. A clear understanding of the working principle of CAN sampling within the MCU is essential for comprehending the practical significance of CAN transceiver timing parameters and for correctly configuring the CAN controller of the MCU. This section will mainly describe the CAN sampling principle in a system and explains it with reference to sampling point tests in the system.

2.1.CAN bit structure

Within the MCU, each CAN bit is divided into several Time Quantum (T_q). The duration of each T_q is determined by the clock frequency allocated to the CAN module. The number of T_q per bit is then set according to the desired CAN communication baud rate. In practice, the communication rate and the number of T_q per bit are typically defined first, followed by clock configuration to meet these requirements.

For example:

If the system clock, after prescaling, provides the CAN module with a 40 MHz clock, then the duration of each T_q is 1/40 MHz = 25 ns. If the communication data rate is 500 kbps (bit time = 2 µs) for both the Arbitration Field and the Data Field, the number of T_q per CAN bit is 2000 ns / 25 ns = 80. For a CAN FD with a Data Field rate of 2 Mbps (bit time = 500 ns), the number of T_q per CAN bit is 500 ns / 25 ns = 20.

As illustrated in Figure 2.1, a CAN bit composed of multiple T_q is further subdivided into several functional segments: Synchronization Segment (SS), Propagation Time Segment (PTS), Phase Buffer Segment 1 (PBS1), and Phase Buffer Segment 2 (PBS2). In many MCUs, it is also common to see PTS and PBS1 are combined into Time Segment 1 (TSEG1), while PBS2 is referred to as Time Segment 2 (TSEG2). Additionally, due to the resynchronization mechanism, the concept of reSynchronization Jump Width (SJW) is introduced.

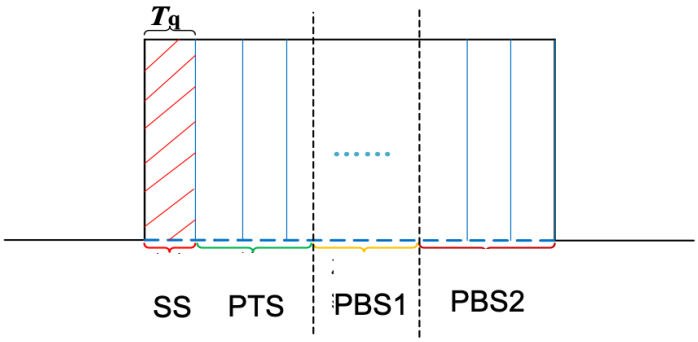


Figure 2.1 CAN bit structure definition

Typically, SS occupies 1 T_q. The number of T_q for TSEG1 and TSEG2 is determined based on the desired sampling point location and the propagation delay compensation requirements. The SJW must be less than that of both PBS1 and PBS2. The sampling point generally placed at the end of PBS1. The sampling point position is calculated as:
Sample Point Position (%) = [Length of SS + Length of TSEG1 (PTS + PBS1)] / Total Number of T_q per Bit * 100%

2.2.Synchronization

CAN clock synchronization consists of two mechanisms: hard synchronization and resynchronization. In a multi-node system, clock frequency deviations of each ECU and phase delays along the transmission path can cause timing misalignment. Therefore, the receiving ECU needs to adjust its reception timing through hard synchronization and resynchronization to ensure normal communication at the node.

Hard synchronization occurs at the Start-of-Frame (SOF) bit of the transmitting node, where the falling edge of the SOF lies within the SS of the transmitting node's bit. The receiving node, based on the detected falling edge of the received SOF bit, aligns its sampling SS to this position, achieving synchronization between the transmitting and receiving nodes, as shown in Figure 2.2.

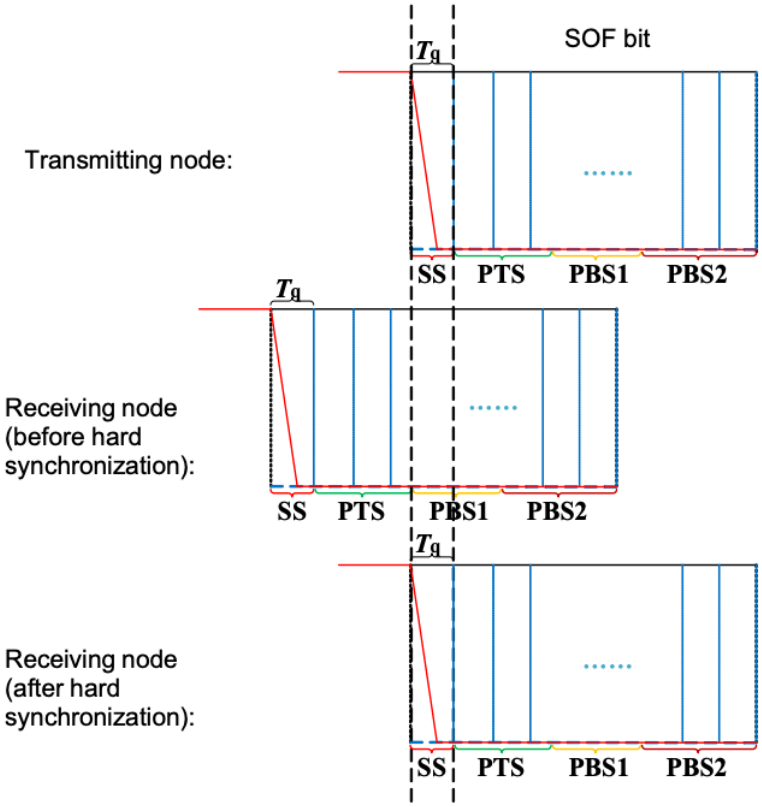


Figure 2.2 Schematic of hard synchronization

Resynchronization occurs at every subsequent falling edge within the CAN frame after the hard synchronization at the SOF bit. Ideally, after hard synchronization, the falling edges of the CAN bits from both the transmitting and receiving nodes will fall within the SS. However, due to factors like propagation path phase delays, the receiver's bit timing will misalign with the transmitter's over time, potentially leading to sampling errors. Therefore, corrections via resynchronization are required. During resynchronization, if the bit's falling edge is detected before the SS of the receiving node, the receiver will reduce the number of T_q in PBS2 to ensure alignment of the receiver's sampling point position (relative to SS) with the transmitter for synchronization. If the bit's falling edge is detected after the SS of the receiving node, the receiver will increase the number of T_q in PBS1 to achieve synchronization. The actual number of T_q adjusted does not exceed the SJW value. Resynchronization is illustrated in Figure 2.3.

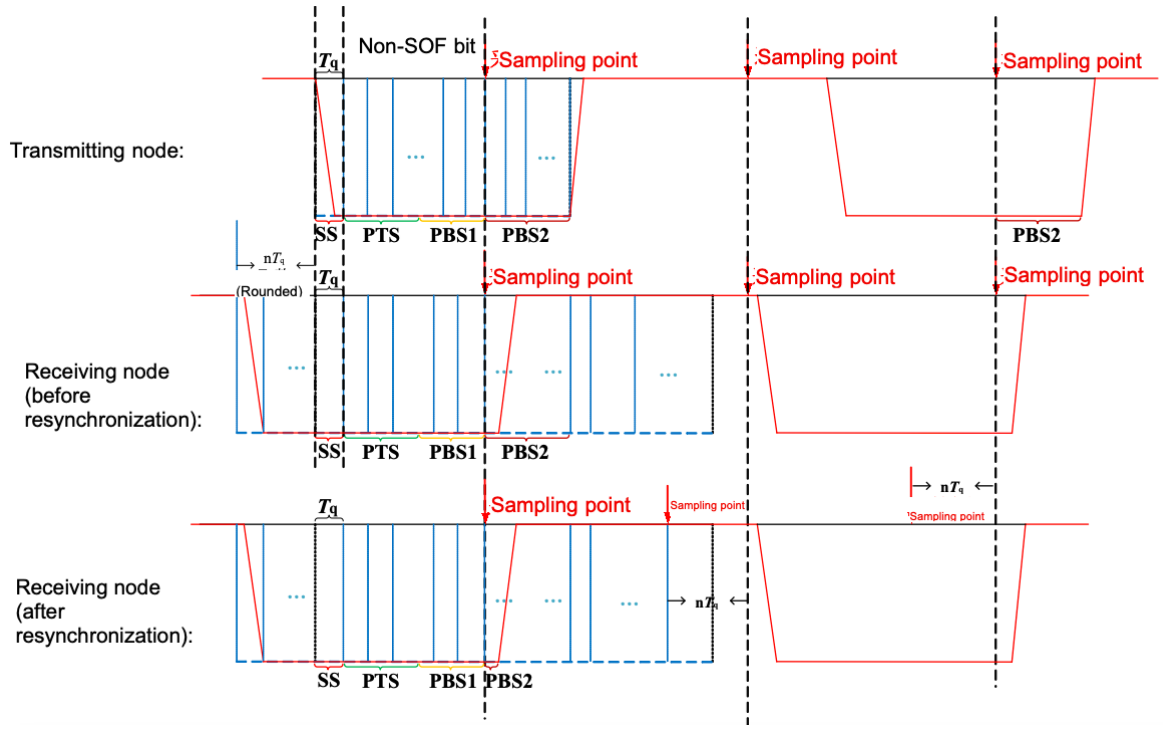


Figure 2.3 resynchronization diagram

2.3.Propagation delay compensation

In a typical CAN system, there are two main sources of propagation delay: loopback delay and round-trip delay from the transmitting node to the receiving node and back to the transmitting node, as illustrated in Figure 2.4.

The loopback delay (Delay1) includes delay from the MCU's TXD output to the transceiver's TXD input, the intrinsic loop delay of the CAN transceiver, and delay from the transceiver's RXD output to the MCU's RXD input.

The delay from the transmitting node to the receiving node (Delay2) includes: internal transmission delay within the transmitting MCU, delay from the MCU's TXD pin to the transceiver's TXD pin, internal transmission delay within the transceiver, propagation delay from transceiver's bus pin to transceiver's bus pin (including PCB traces and physical bus), internal reception delay within the transceiver, delay from the transceiver's RXD pin to the receiving MCU's RXD pin, and internal reception delay within the receiving MCU. The propagation delay from the receiving node back to the transmitting node (Delay3) is approximately equal to Delay2.

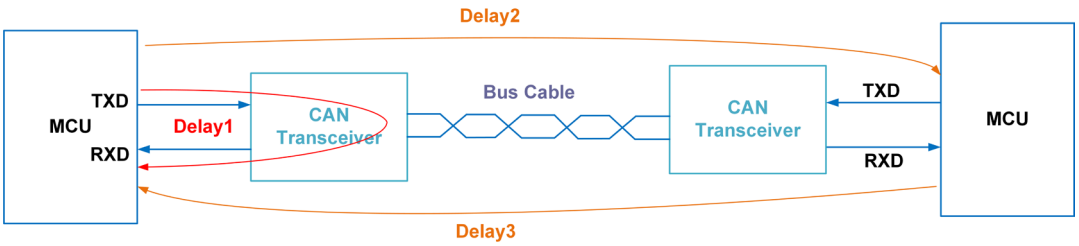


Figure 2.4 propagation delays diagram

The CAN protocol requires that a transmitting node simultaneously monitor the signals returned by the bus. If the transmitted data does not match the received data (except the Arbitration Field), a transmission error will be reported. Additionally, after successfully transmitting a CAN frame, the transmitting node is required to send two ACK bits. Upon acknowledging correct signals received, the receiving node will respond to the first ACK bit (also called the ACK slot) by overriding the recessive bit with a dominant bit. The transmitting node, upon sampling a dominant bit in the ACK slot, considers CAN frame transmission successful. If no dominant level is detected, the transmitting node will assume a transmission error.

These CAN protocol rules necessitate that the PTS in the bit timing must be longer than either Delay1 or the sum Delay2 + Delay3. This ensures that the transmitting node can correctly sample the signal without error. For CAN self-transmit and self-receive scenarios, ISO11898-2 specifies a maximum loop delay of 255 ns. For a traditional CAN frame at 500 kbps, where the bit time is 2 µs, the PTS can easily be configured to exceed 255 ns, ensuring reliable signal sampling. However, for CAN FD (up to 5 Mbps, bit time = 200 ns) and for CAN SIC (up to 8 Mbps, bit time = 125 ns), the bit time becomes shorter than the propagation delay. In such cases, relying solely on the PTS is insufficient to compensate for the propagation delay (as shown in Figure 2.5), leading to sampling errors and communication failures.

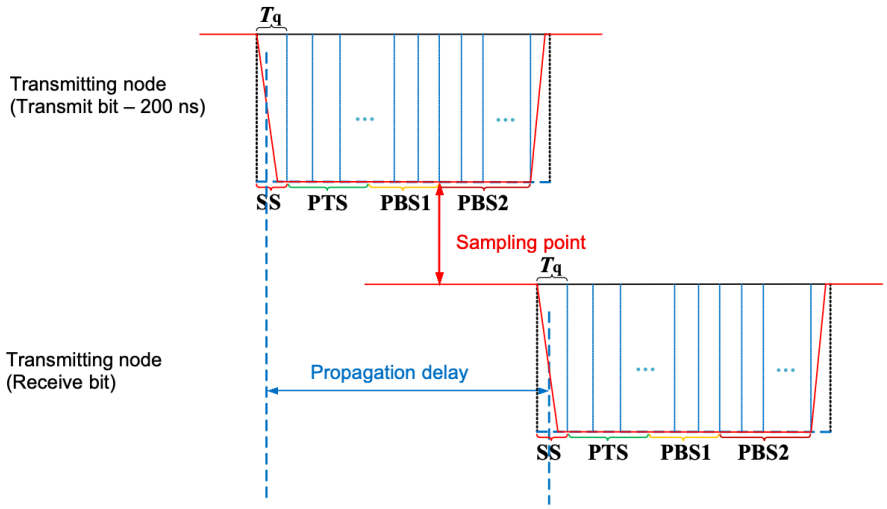


Figure 2.5 uncompensated propagation delay in CAN FD @ 5 Mbps diagram

To address the challenge in CAN FD where the high communication rate makes the PTS insufficient for delay compensation, CAN FD incorporates a Transceiver Delay Compensation (TDC) mechanism. This introduces a Second Sampling Point, as shown in Figure 2.6.

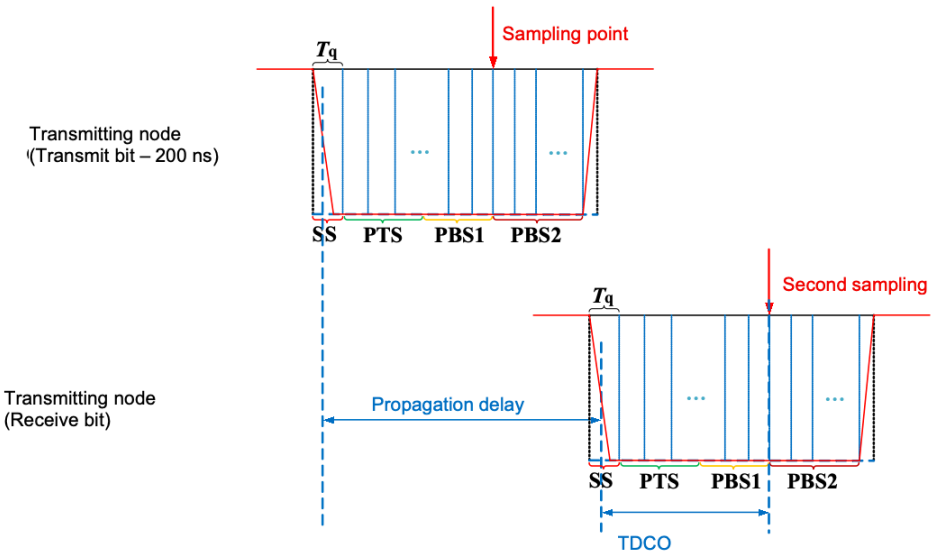


Figure 2.6 propagation delay compensation in CAN FD @ 5 Mbps (Second Sampling Point) diagram

In CAN FD communication, when TDC is enabled, the CAN controller will automatically measure the Transceiver Delay Compensation Value (TDCV) between the falling edge from the FDF bit to the r0 bit on its TXD pin and the corresponding falling edge on the RXD pin. Based on the current T_q duration, the number of T_q to compensate is calculated (TDCV / T_q). The Transceiver Delay Compensation Offset (TDCO) is typically set to align with the nominal sampling point location. Consequently, the final position of the second sampling point, relative to the original falling edge of the transmitted bit, is TDCV + TDCO. This ensures accurate sampling by the CAN controller during the CAN FD communication. Finally, it is important to note that the second sampling point is only used under the transmitting node's self-transmit and self-receive mode, and that it does not apply when the node is receiving messages from other nodes on the bus.

2.4.Common issues in sampling point test

Sample point test is an essential item when carrying out CAN transceiver tests in a system. The primary purpose of this test is to verify whether the configured CAN sampling point position in the MCU meets requirements during actual communication. The test setup is shown in Figure 2.7.

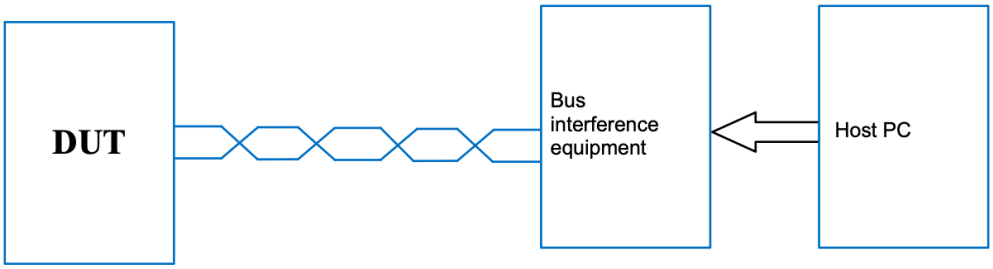


Figure 2.7 Sampling point test setup

As shown in the figure above, the sampling point test method typically involves using a bus interference equipment to generate a CAN frame where a specific bit is interfered, which is transmitted to the Device Under Test (DUT). The timing of the interfered bit in the CAN frame is progressively altered until the DUT detects error in the received frame. It then transmits the errored frame back to the bus interference equipment, which reports the error. The current sampling point position of the DUT is calculated and displayed on the host PC. A commonly used bus interference equipment is the Vector VH6501, which operates at a maximum system clock frequency of 160 MHz and can apply a minimum interference time of 6.25 ns. It works by applying an interference that overwrites a specific dominant bit in the CRC field with a recessive level, starting from the end of the bit and moving forward, thereby increasing the length of the subsequent recessive bits while keeping the total bit length unchanged. The VH6501's sampling point (configured to be earlier than the DUT's expected sampling point to ensure the DUT detects the error first) and the CAN module clock are pre-configured. The specific test method is illustrated in Figure 2.8.

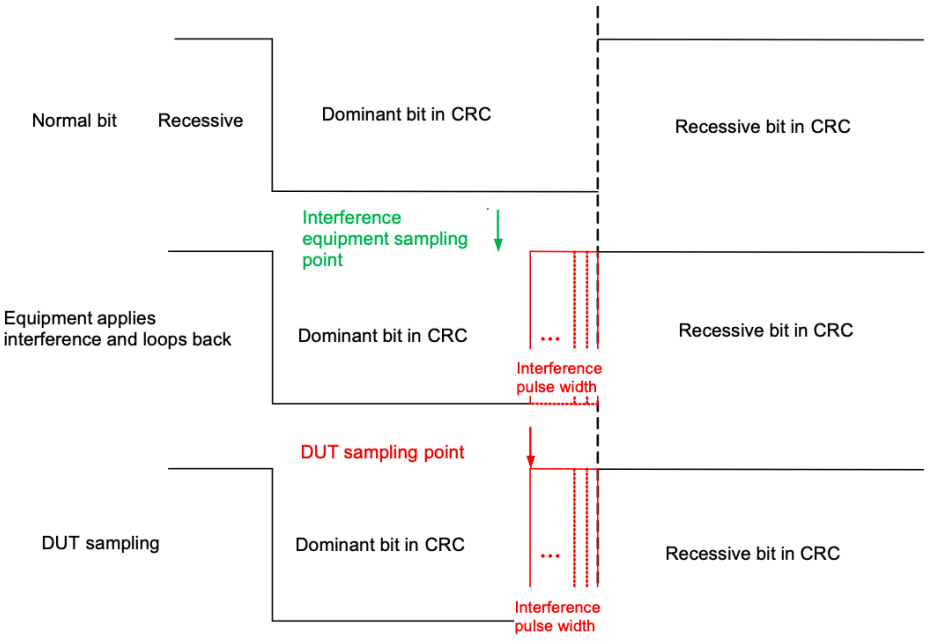


Figure 2.8 sampling point test diagram

The sampling point test result for the DUT is obtained by calculating the ratio of the undisturbed pulse width of the dominant bit (when the DUT transmits an error frame) to the total bit length. However, significant deviations often occur in actual tests. For example, with a configured sampling point at 80%, the test result may be 70% or even lower, or sometimes 85% or higher. We have analyzed potential causes of these deviations. In the sampling point test, the CAN frame transmitted by the interference equipment is converted by the transceiver from a differential bus signal to a single-ended signal on the RXD pin. During this process, the bit time can undergo distortion (see $t_{\Delta REC}$ in Section 1), which will affect the accuracy of the test results, as shown in Figure 2.9.

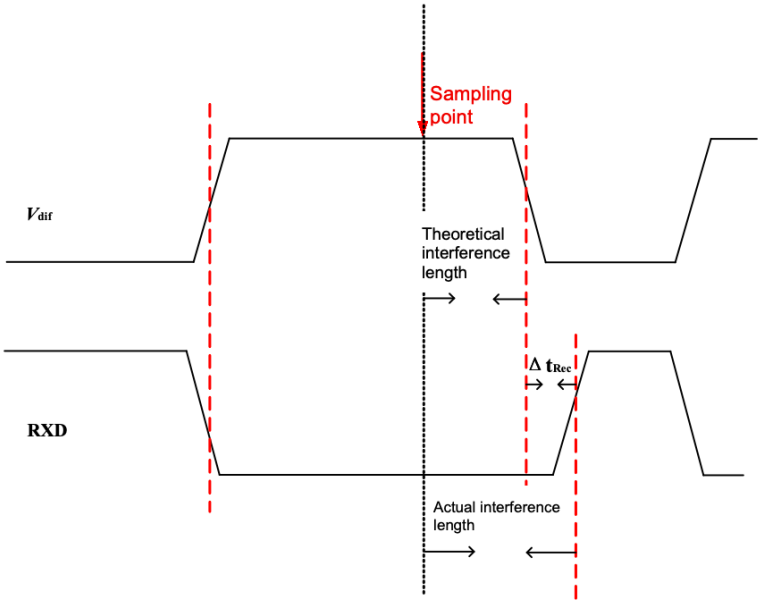


Figure 2.9 Effects of bit time distortion on sampling point test

After the bus signal passes through the transceiver, the bit time can become distorted. The ISO11898-2 standard specifies a Δt_{rec} range of -65 ns to +40 ns for commination rate at 2 Mbps. Consequently, the bit time arriving at the RXD pin can be slightly longer or shorter. This causes the segment length that the interference equipment needs to disturb to either increase or decrease, affecting the accuracy of the test result. It is important to underline that this increase or decrease in the disturbed bit time only affects the result under this specific test method. The distance from the sampling point to the falling edge remains unchanged, and is still the sampling position set in the software (using the falling edge as the reference). Therefore, if the DUT's Δt_{rec} is significant, the error introduced by Δt_{rec} must be considered when interpreting the test results.

Furthermore, due to clock deviations between the DUT and the interference equipment in the test system, plus phase delays in signal transmission, both hard synchronization and resynchronization are active in the DUT. This can lead to cases as shown in Figure 2.10.

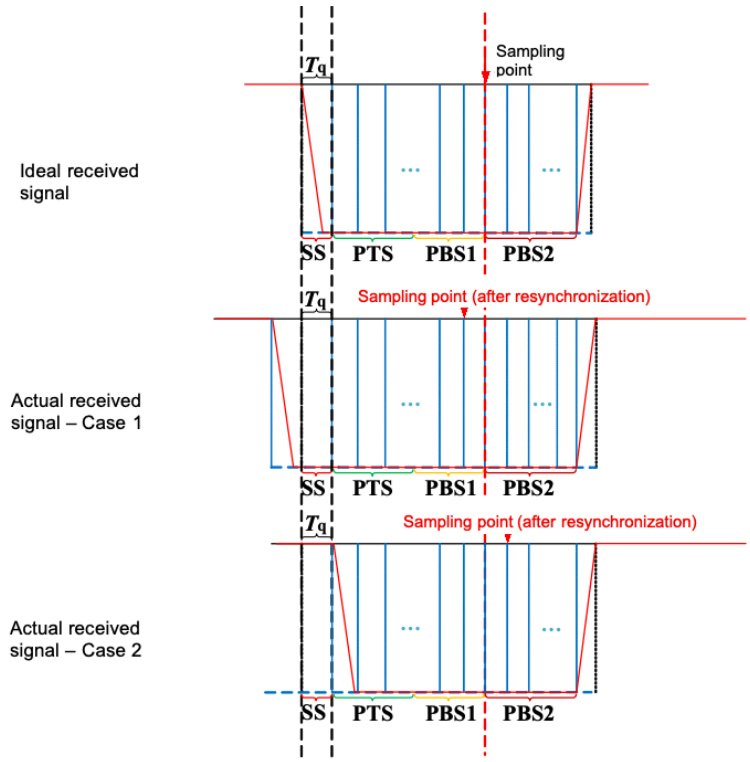


Figure 2.10 Cases of DUT receiving signals during sampling point test

In Case 1, factors like pulse width distortion, phase delay, and clock deviation cause the falling edge before the disturbed bit to arrive one Tq earlier relative to the SS. Due to the resynchronization mechanism, the sampling point will also shift earlier by one T_q. This requires the interference pulse width to be one T_q longer to affect the DUT's sampling point, resulting in a measured sampling point that is one T_q smaller than the configured value. Similarly, in Case 2, if the falling edge arrives one T_q later, resynchronization will shift the sampling point later by one T_q. Consequently, an interference pulse width one T_q shorter is sufficient to affect the DUT's sampling point.

Since the shift of the falling edge relative to the SS accumulates gradually, when the falling edge just slips outside the SS, resynchronization will immediately shift the sampling point forward or backward by one T_q. This can cause a deviation in the sampling point test result. The magnitude of this deviation depends on the T_q duration configured in the DUT's MCU. For a CAN FD system with a bit time of 500ns, if the CAN module clock is configured to 20 MHz, one T_q is 50 ns. Based on the analysis above, the potential sampling point test deviation could be 50 ns / 500 ns * 100% = 10%. If the CAN module clock is configured to 40 MHz, one T_q is 25 ns, leading to a potential deviation of 25 ns / 500 ns * 100% = 5%. Therefore, for sampling point test in a system, the configuration of the MCU's T_q count has a significant impact. Additionally, the transceiver's pulse width distortion also influences the sampling point test result. Different pulse width distortion time durations under the same setup may yield different test results. Increasing the number of T_q can, to some extent, converge the test results and mitigate variations in sampling point test results caused by differences in pulse width distortion time. Section 1 provides comparative data for NOVOSENSE's CAN transceivers benchmarked against major international manufacturers regarding receive bit time distortion. The results were relatively consistent, indicating minimal impact on variations in sampling point test results.

3.Effects of CAN Dynamic Parameters on Systems

Sections 1 and 2 provide the definitions of CAN-related dynamic parameters, comparative test data, and the fundamental working principle of CAN sampling. These parameters have a significant impact on normal CAN communication in real-world systems. This section will detail the effects of CAN dynamic timing parameters on system communication.

- Rise/fall time

When the rising or falling edge of the CAN transceiver's output bus differential signal is relatively slow, it can lead to shortened bit time after conversion by the transceiver, as illustrated in Figure 3.1.

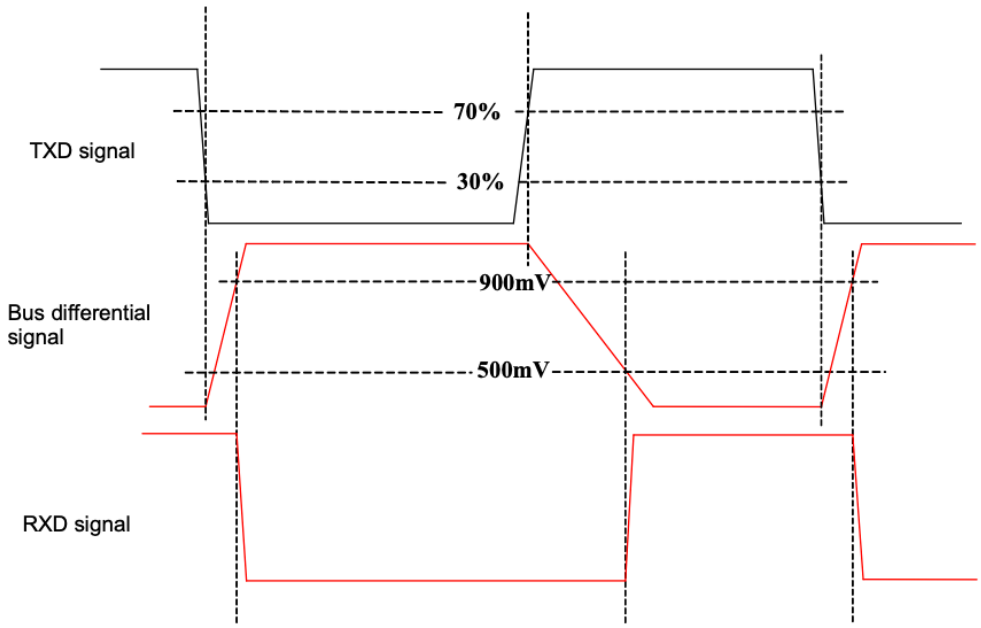


Figure 3.1 Schematic of slow bus differential signal falling edge

As shown in the figure above, a slow falling edge of the bus differential signal can cause the dominant bit time on the RXD output (after conversion by the CAN transceiver from the TXD input) to be extended and the recessive bit time shortened. If the dominant bit is lengthened to the sampling point of the subsequent recessive bit, it may lead to incorrect sampling by the MCU, causing CAN communication errors. If the bus differential signal edges are slow but the resulting pulse width distortion remains within acceptable limits (i.e., the impact on the RXD bit time is minimal, unlike the severe impact examples given above), the effects on communication will be negligible.

In real-world applications, CAN communication networks often have long cabling and multiple nodes, leading to significant bus parasitic capacitance which slows down the bus signal edges. However, if the bit timing requirements are still met, communication will not be significantly affected. System design typically imposes limits on the number of CAN nodes and bus length to ensure reliable communication.

The falling edge of the RXD signal is crucial for synchronization. If the falling edge is relatively slow, coupled with edge shifts caused by factors like propagation phase delay, the effective bit time can be reduced. This may exceed the compensation capability of the SJW, which is typically only 2-3 T_q in length, leading to MCU sampling errors and disrupted communication. Therefore, the rise/fall time of the RXD signal should be sufficiently short, ideally ensuring that edges are within one SS.

- Propagation delay

Based on the analysis of the sampling principle in Section 2, we know that propagation delay compensation is required for applications with high CAN communication rates. For the ACK response scenario, according to ISO11898, the fastest bit rate for the ACK field is 1 Mbps, corresponding to a bit time of 1 µs. The system needs to sample the dominant ACK bit from the remote node at the configured sampling point within this 1 µs window (depending on the sampling point position, typically allowing 700-800+ ns). Therefore, the sum Delay2 + Delay3 must be less than this available sampling window. This requirement is generally met in most applications. For some special system applications, where the physical transmission line introduces significant propagation delay, the internal delay of the transceiver needs to be as short as possible to compensate for the system-level delay and ensure reliable communication (in applications with very long transmission lines, the CAN communication rate is usually reduced).

For the self-transmit and self-receive scenario, if the propagation delay measured by the MCU exceeds the maximum compensable range, the TDC function will fail. This results in sampling errors and prevents normal CAN communication. The delay measured by the MCU includes not only the CAN transceiver's propagation delay but also delays from PCB traces and the MCU's internal paths. Therefore, ensuring a low propagation delay for the CAN transceiver across different operating environments is crucial, as it provides sufficient margin for the system to meet the propagation delay compensation requirements.

- Bit time and bit time distortion

Bit time transmission distortion causes the bus bit time and the RXD bit time to increase or decrease. Here, we combine the influences of these two parameters as the effect of CAN bit time variation on system. Ultimately, both TXD-to-bus and bus-to-RXD bit time distortions manifest as an increase or decrease in the bit time observed on the RXD signal. The impact on sampling point test was discussed in Section 2.4. If the bit time on RXD is significantly larger or smaller than the bit time transmitted from TXD, and considering also the edge shifts, the sampling point (after resynchronization) might sample an incorrect bit state, as shown in Figure 3.2. Therefore, it is required that the bit time distortion of the RXD signal from the transceiver should be small relative to the TXD bit time.

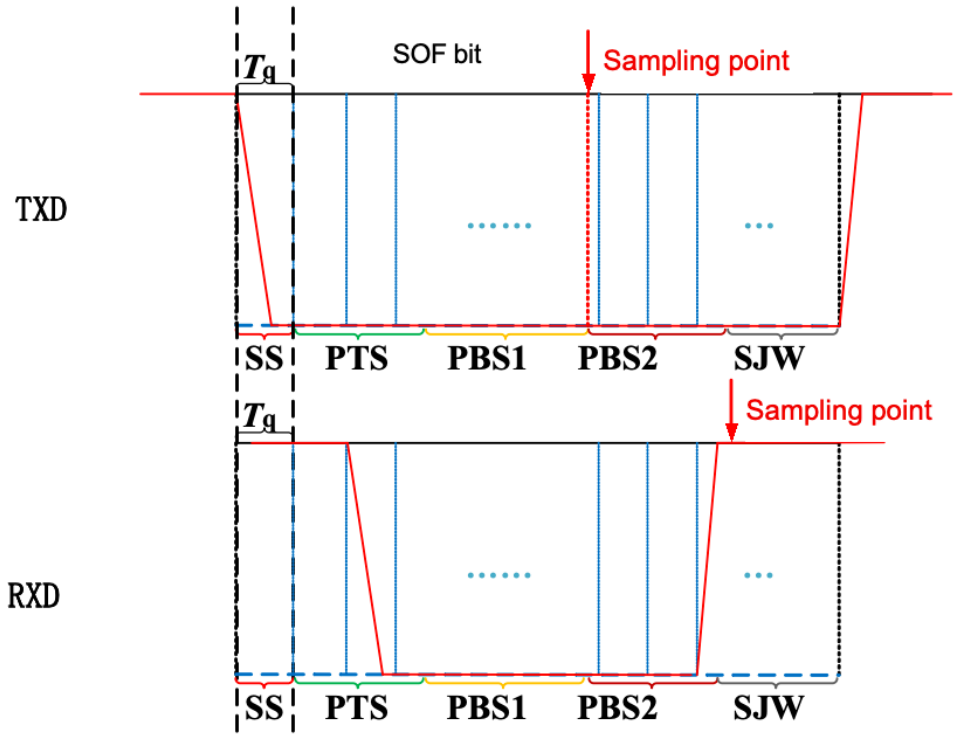


Figure 3.2 sampling with reduced RXD bit time diagram

In summary, the main impact of CAN dynamic parameters is that parameters which do not meet the standard, or are close to the critical value, can lead to incorrect sampling of the RXD signal by the MCU in certain system applications, ultimately resulting in communication failures.

4.Revision History

Revision	Description	Author	Date
1.0	Initial version	Lele Zhang， Fuming Deng	2025/11/12

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